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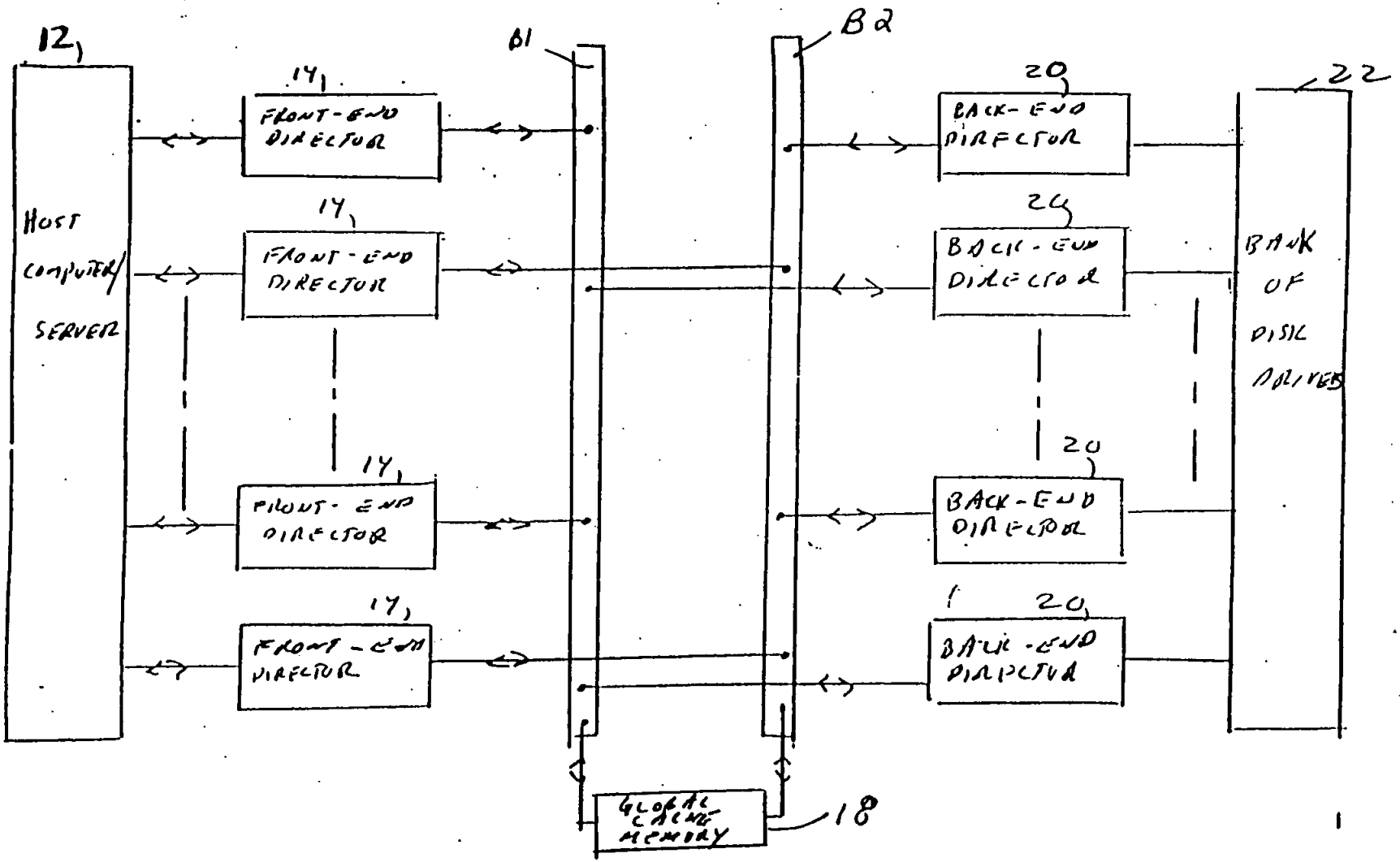
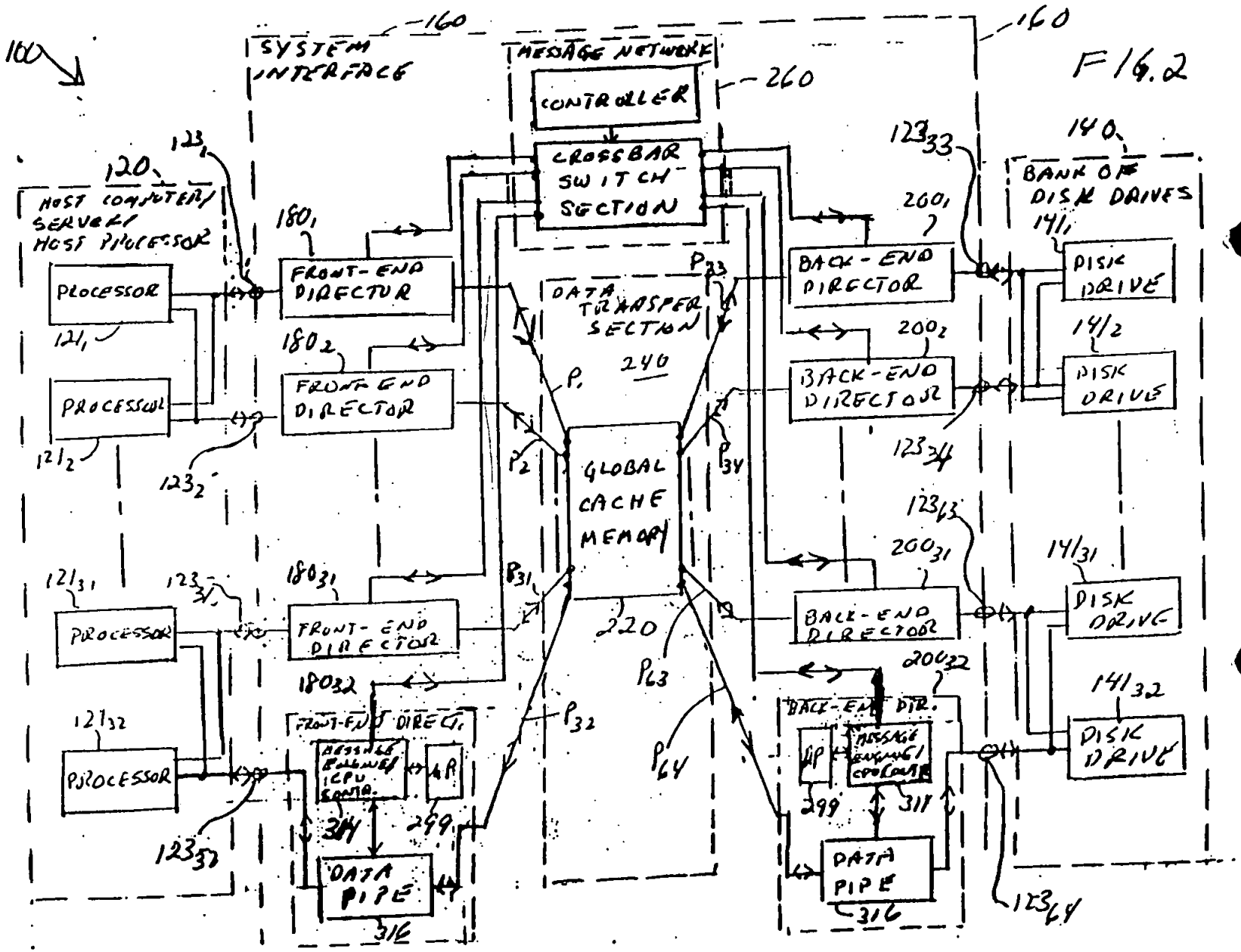
FIG. 1
PRIOR ART




100
SYSTEM INTERFACE
160
MESSAGE NETWORK
CONTROLLER
260
CROSSBAR SWITCH SECTION
120
HOST COMPUTER/ SERVER/ HOST PROCESSOR
PROCESSOR
PROCESSOR
PROCESSOR
PROCESSOR
FRONT-END DIRECTOR
FRONT-END DIRECTOR
FRONT-END DIRECTOR
FRONT-END DIRECTOR
DATA TRANSFER SECTION
240
GLOBAL CACHE MEMORY
220
BACK-END DIRECTOR
BACK-END DIRECTOR
BACK-END DIRECTOR
BACK-END DIR.
DATA PIPE
DATA PIPE
140
BANK OF DISK DRIVES
DISK DRIVE
DISK DRIVE
DISK DRIVE
DISK DRIVE
F16.2

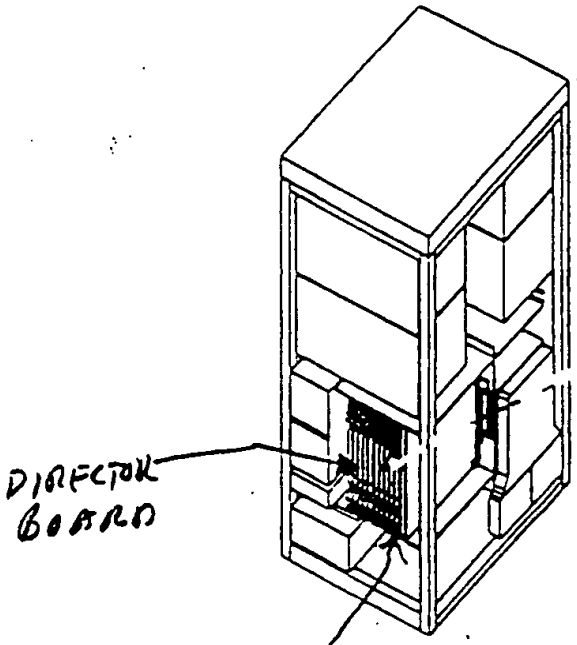
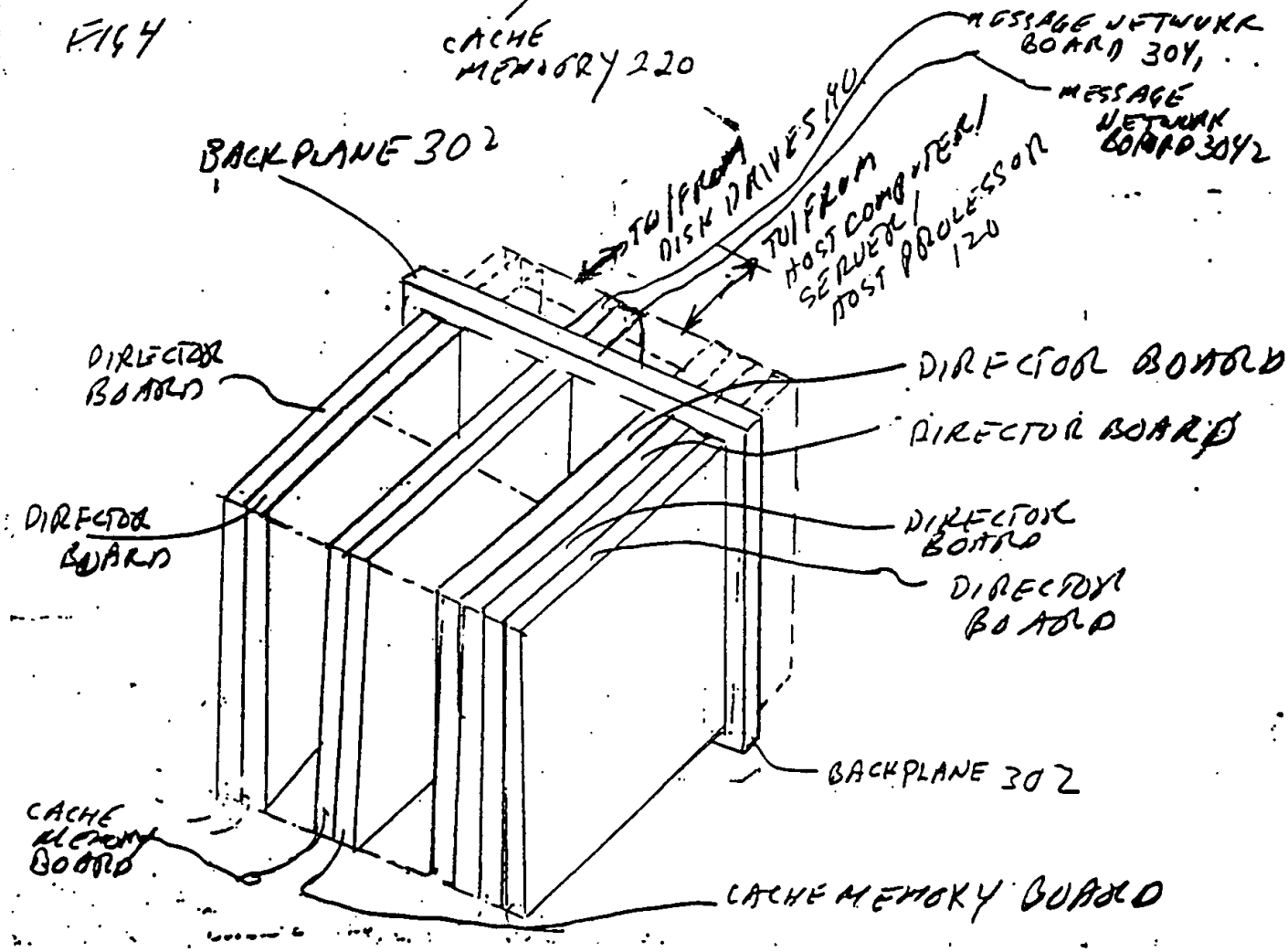
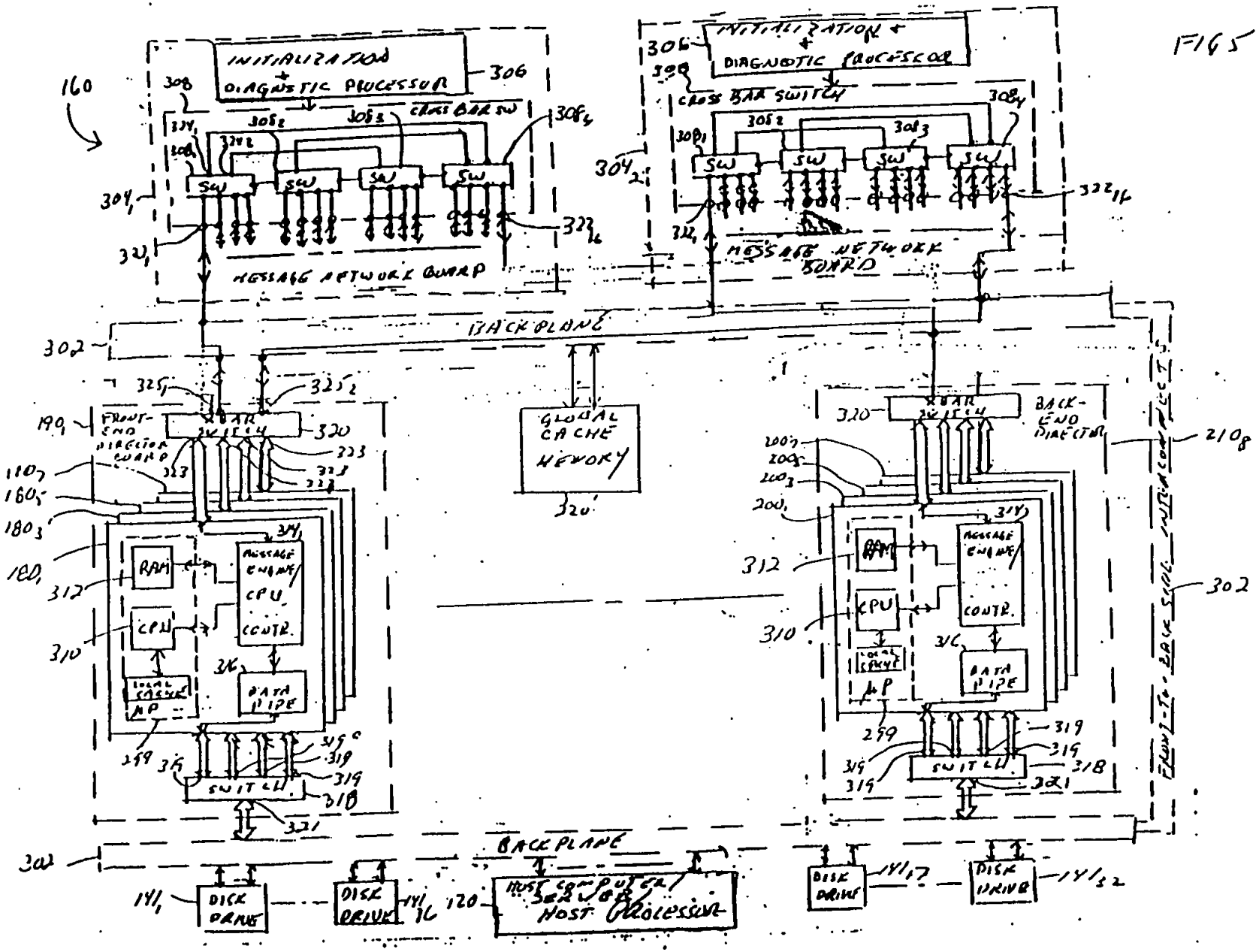

DIRECTOR BOARD
CACHE MEMORY 220

FIG. 3

FIG 4


MESSAGE NETWORK BOARD 304,
MESSAGE NETWORK BOARD 304₂
BACKPLANE 302
TO/FROM DISK DRIVES 140
TO/FROM HOST COMPUTER/ HOST PROCESSOR 120
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
BACKPLANE 302
CACHE MEMORY BOARD
CACHE MEMORY BOARD



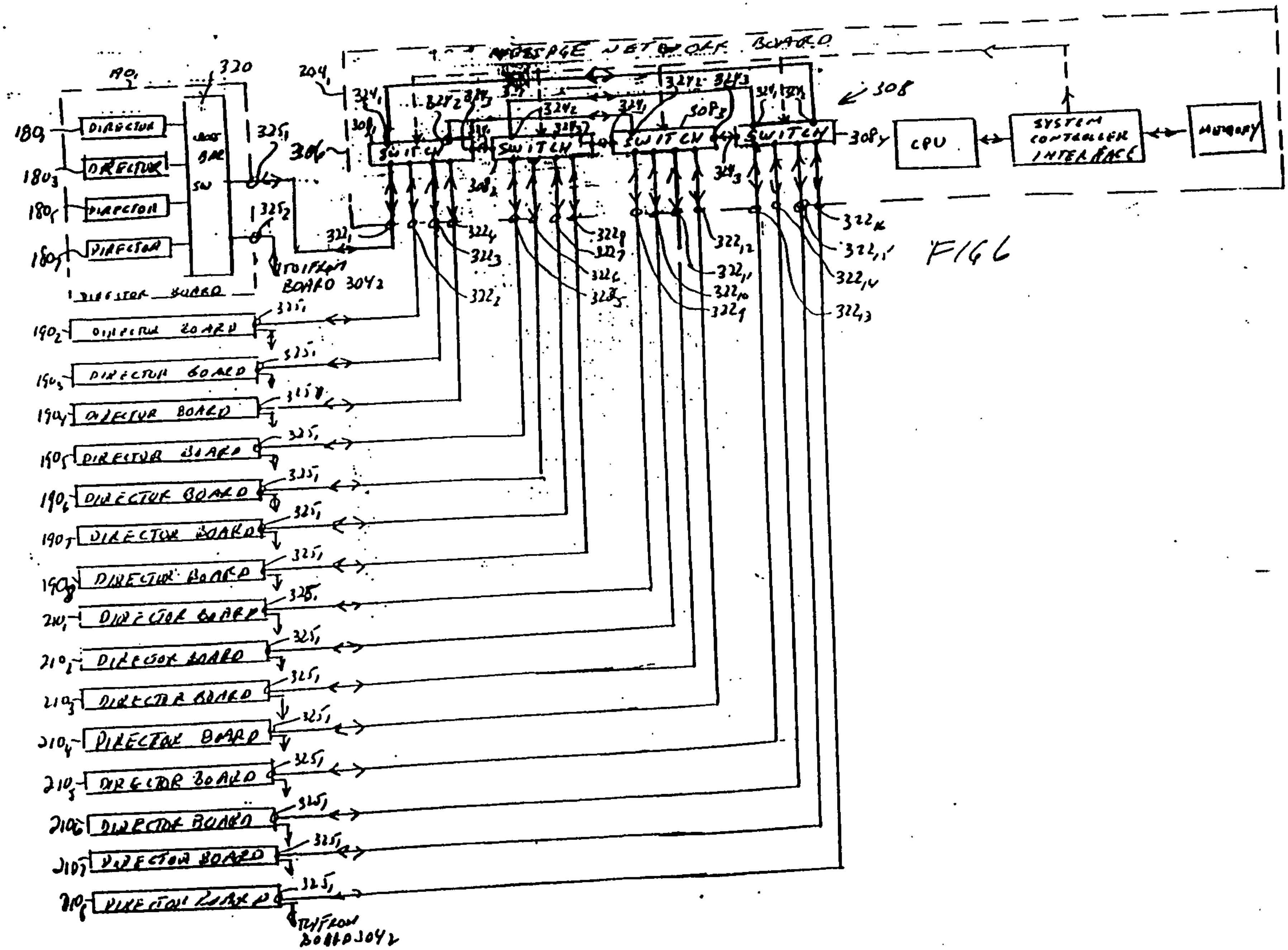
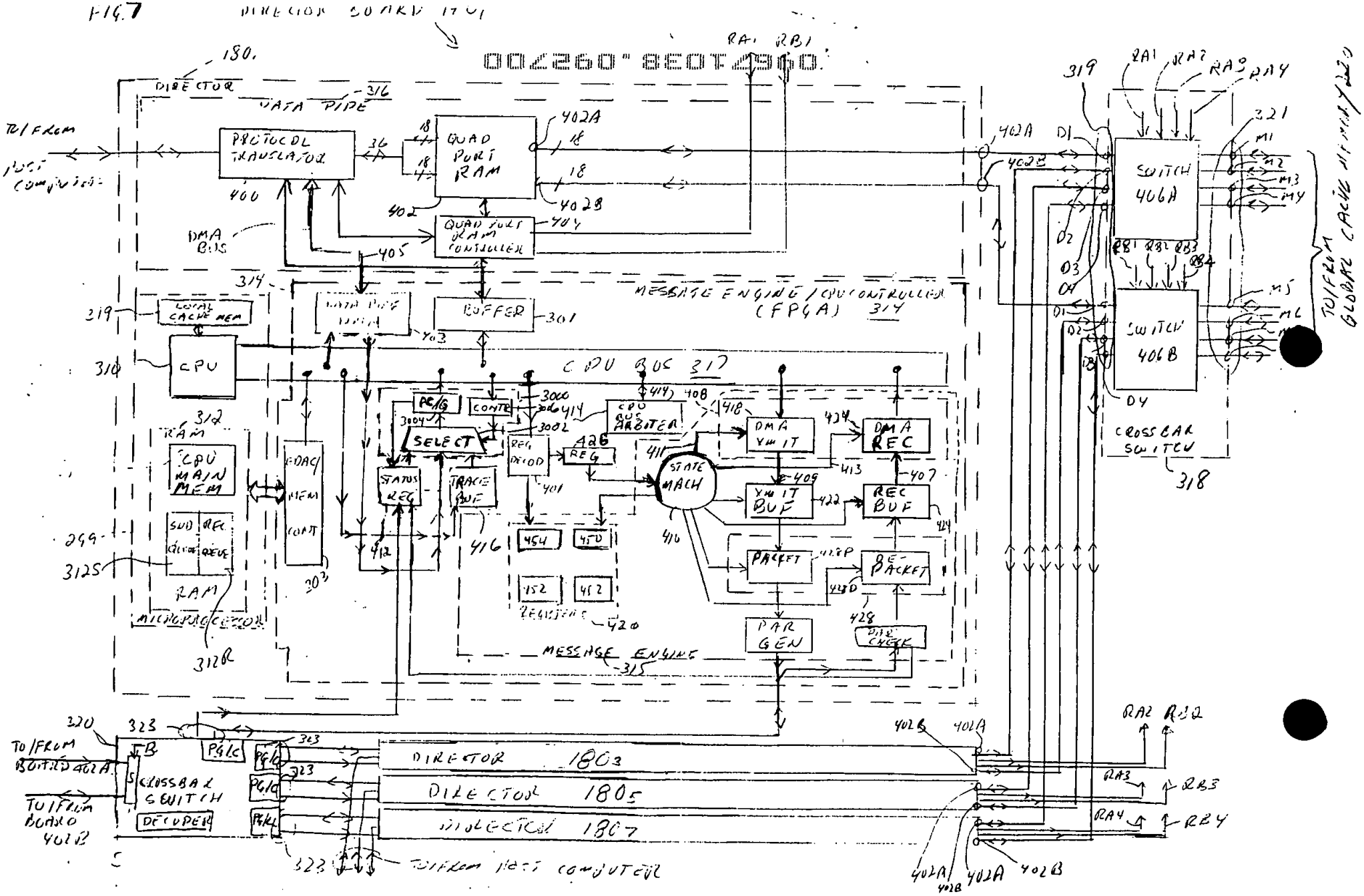
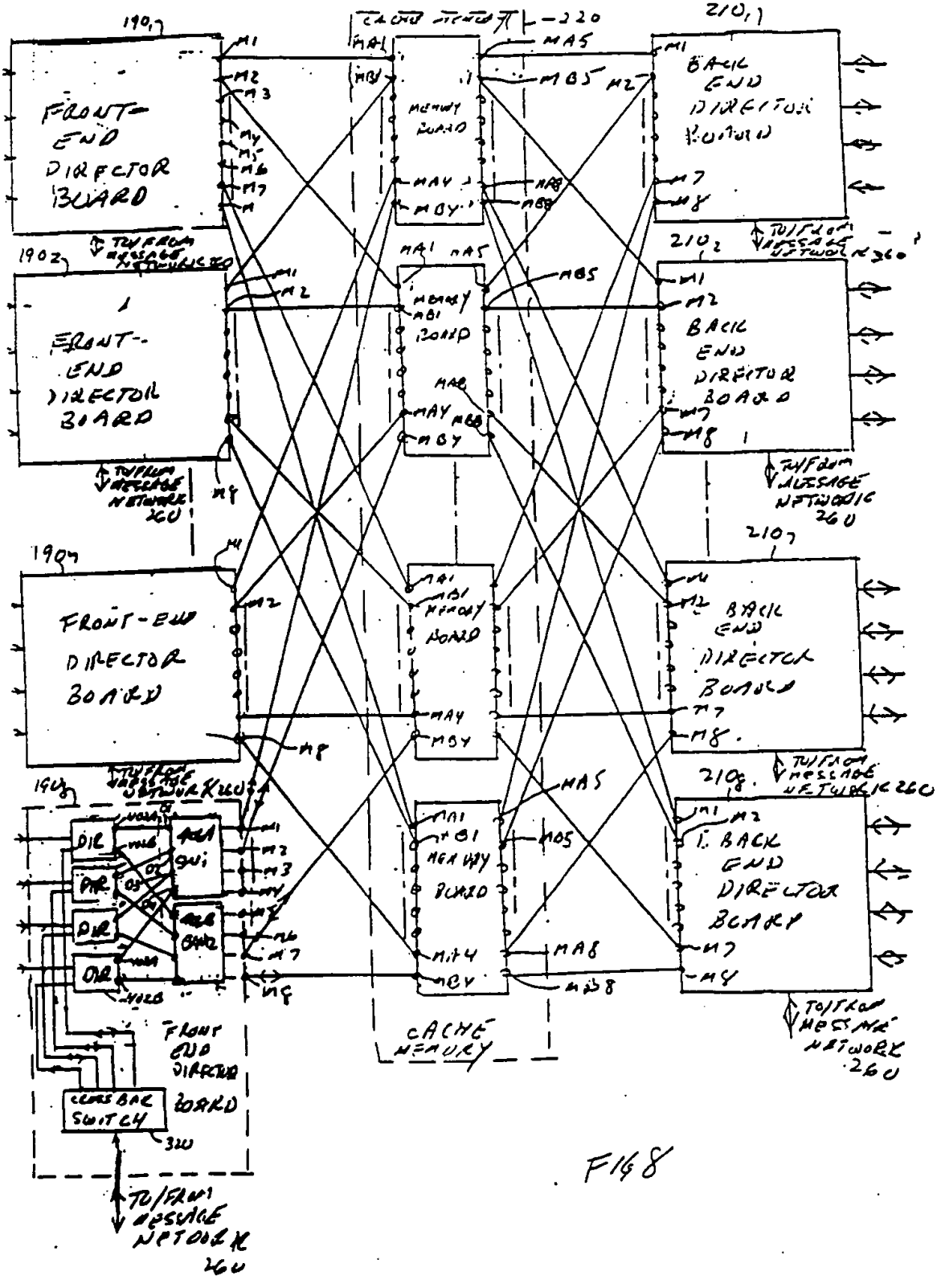

MESSAGE NETWORK BOARD
SWITCH
SWITCH
SWITCH
SWITCH
CPU
SYSTEM CONTROLLER INTERFACE
MEMORY
308
DIRECTOR
DIRECTOR
DIRECTOR
DIRECTOR
SW
DIRECTOR BOARD
TO/FROM BOARD 304₂
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
TO/FROM BOARD 304₂

FIG 6

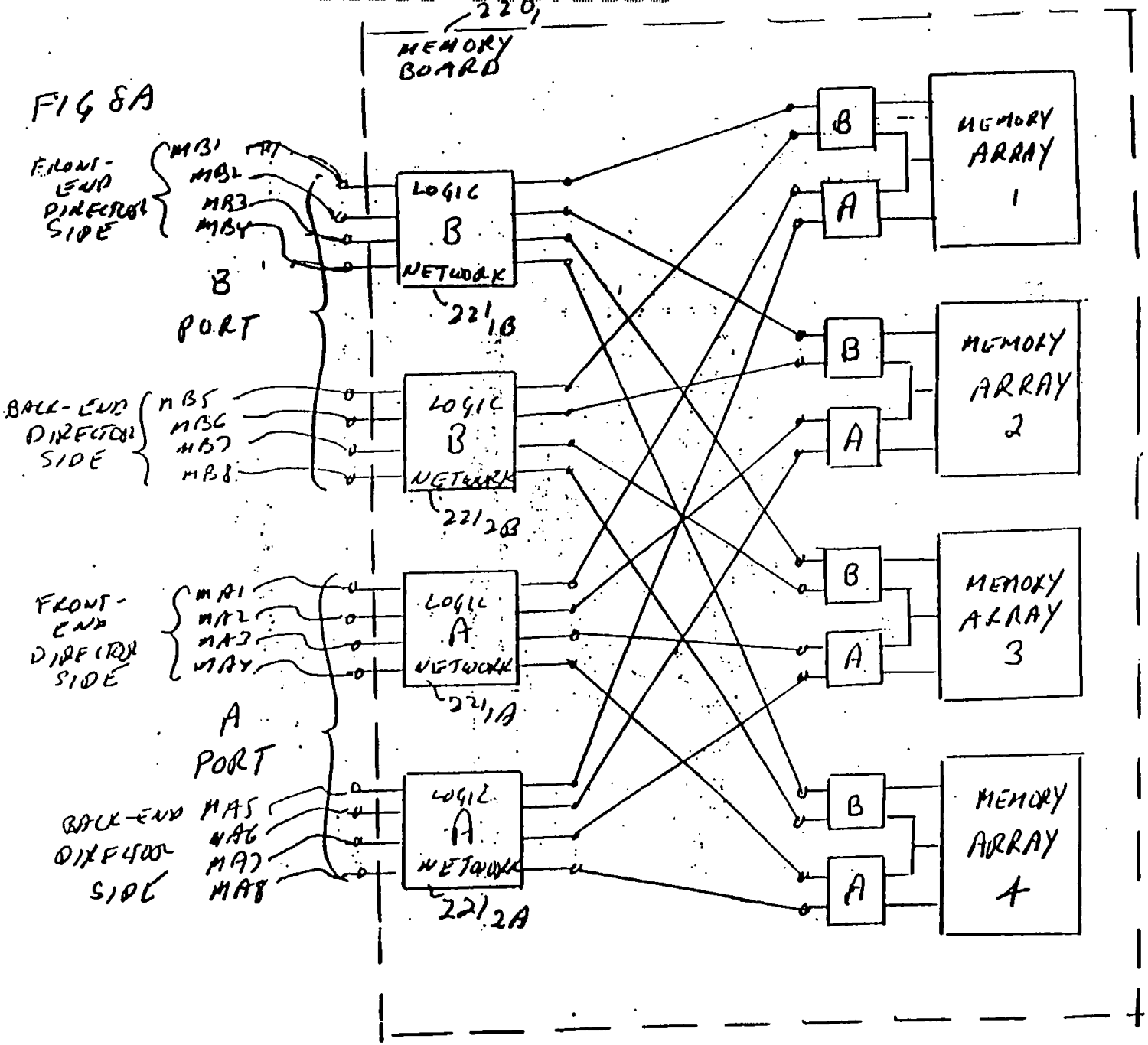
FIG. 7


DIRECTOR BOARD 180
180
DIRECTOR
DATA PIPE 316
TO/FROM HOST COMPUTER
PROTOCOL TRANSLATOR
QUAD PORT RAM
QUAD PORT RAM CONTROLLER
DMA BUS
MESSAGE ENGINE / CPU CONTROLLER (FPGA) 314
LOCAL CACHE MEM
CPU
CPU BUS 317
RAM 312
CPU MAIN MEM
EDAC MEM CONT
SELECT
STATUS REG
TRACE BUF
REG PERIOD
REG
CPU BUS ARBITER
STATE MACH
DMA XMIT
DMA REC
XMIT BUF
REC BUF
PACKET
RE-PACKET
PAR GEN
DATA CHECK
REGISTERS 420
MESSAGE ENGINE 315
MICROPROCESSOR
RAM
SWITCH 406A
SWITCH 406B
CROSSBAR SWITCH 318
TO/FROM GLOBAL CACHE MEMORY
CROSSBAR SWITCH
DECODER
DIRECTOR 1803
DIRECTOR 1805
DIRECTOR 1807
TO/FROM HOST COMPUTER


FRONT-END DIRECTOR BOARD
MEMORY BOARD
BACK END DIRECTOR BOARD
CACHE MEMORY
CROSSBAR SWITCH
TO/FROM MESSAGE NETWORK 26U

F168

FIG 8A



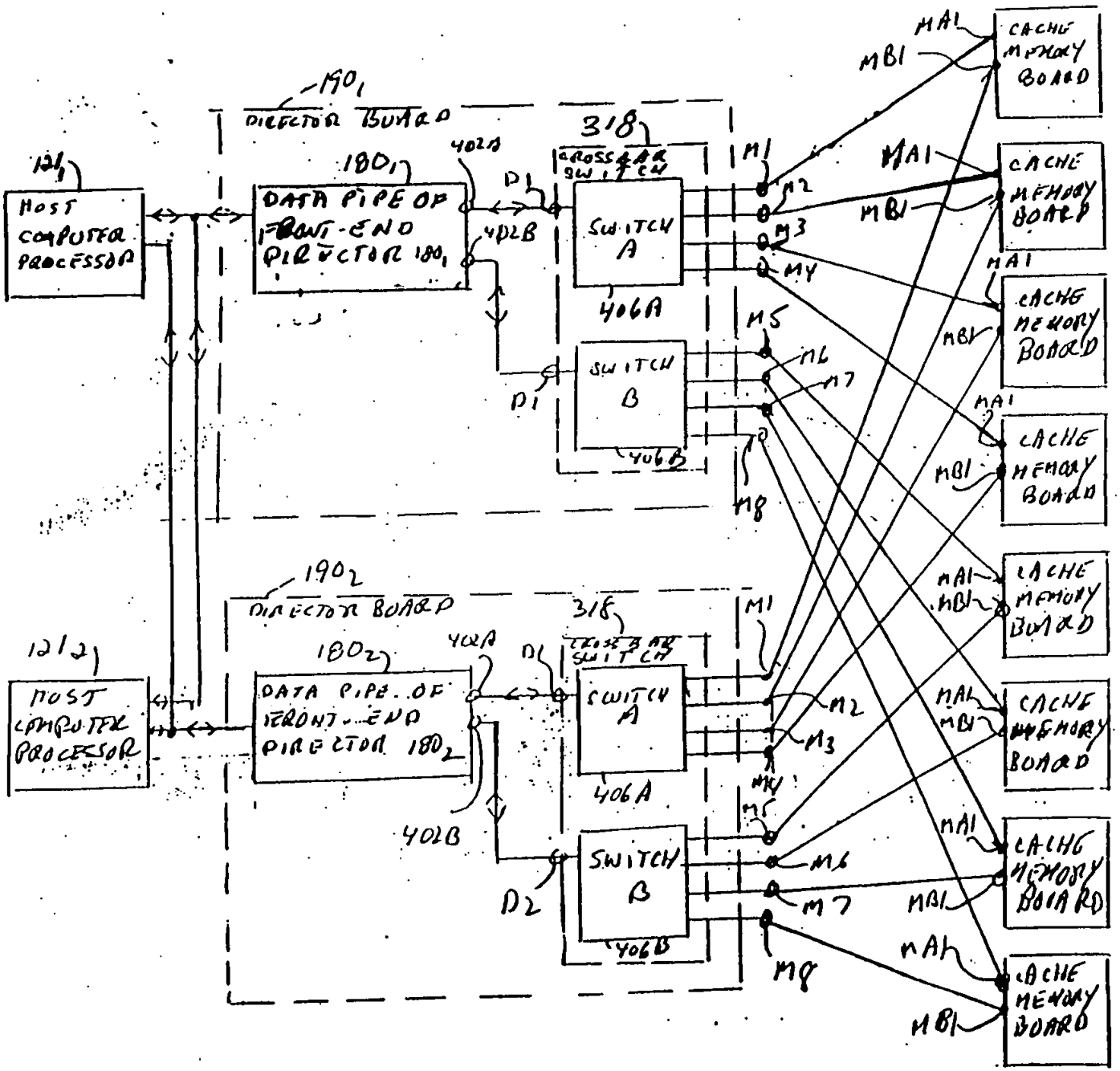

190₁
DIRECTOR BOARD
318
CROSSBAR SWITCH
121₁
HOST COMPUTER PROCESSOR
180₁
DATA PIPE OF FRONT-END DIRECTOR 180₁
402A
402B
D1
SWITCH A
406A
SWITCH B
406B
M1
M2
M3
M4
M5
M6
M7
M8
MA1
MB1
CACHE MEMORY BOARD
190₂
DIRECTOR BOARD
121₂
HOST COMPUTER PROCESSOR
180₂
DATA PIPE OF FRONT-END DIRECTOR 180₂
D2

FIG 8B

FIG. 8C

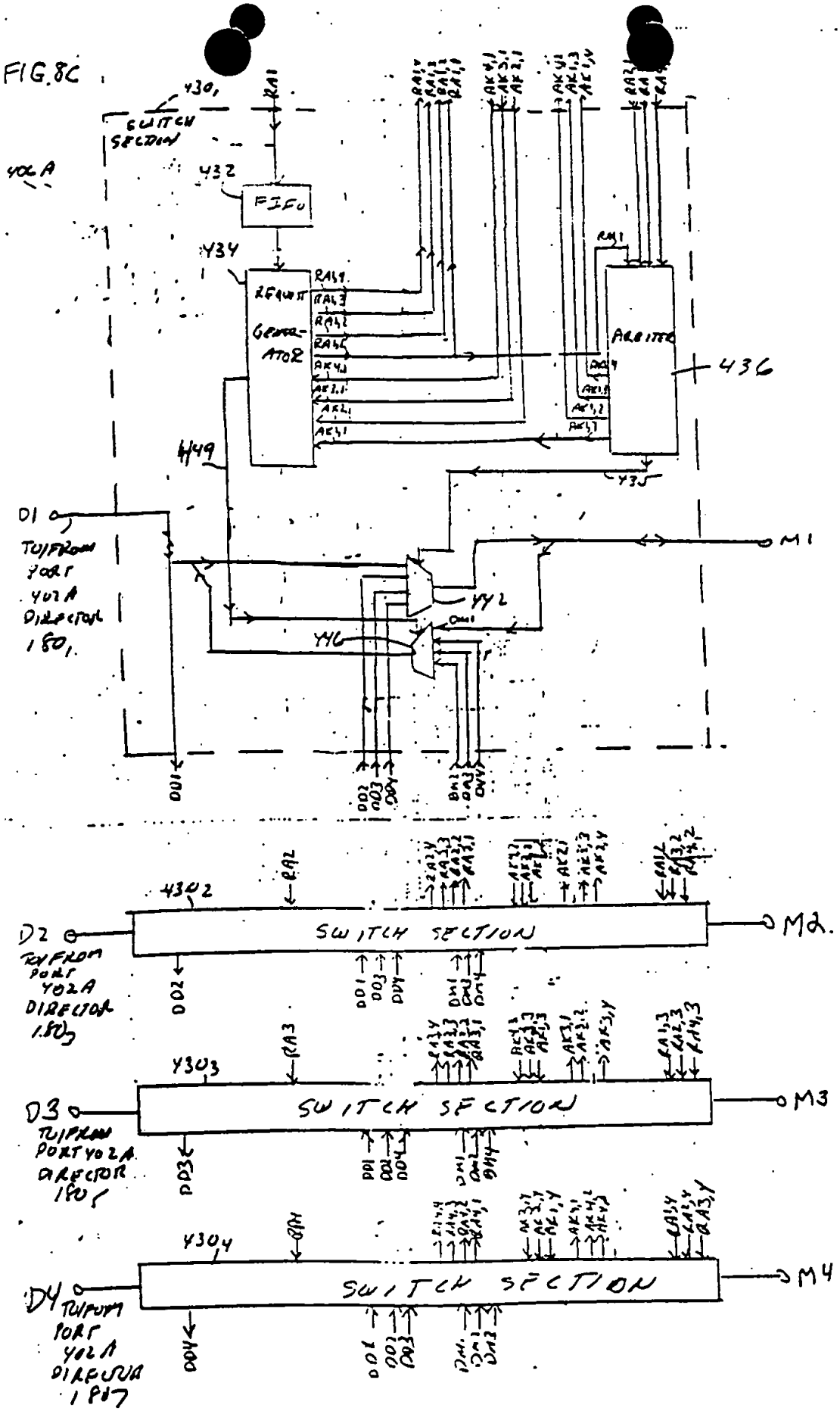
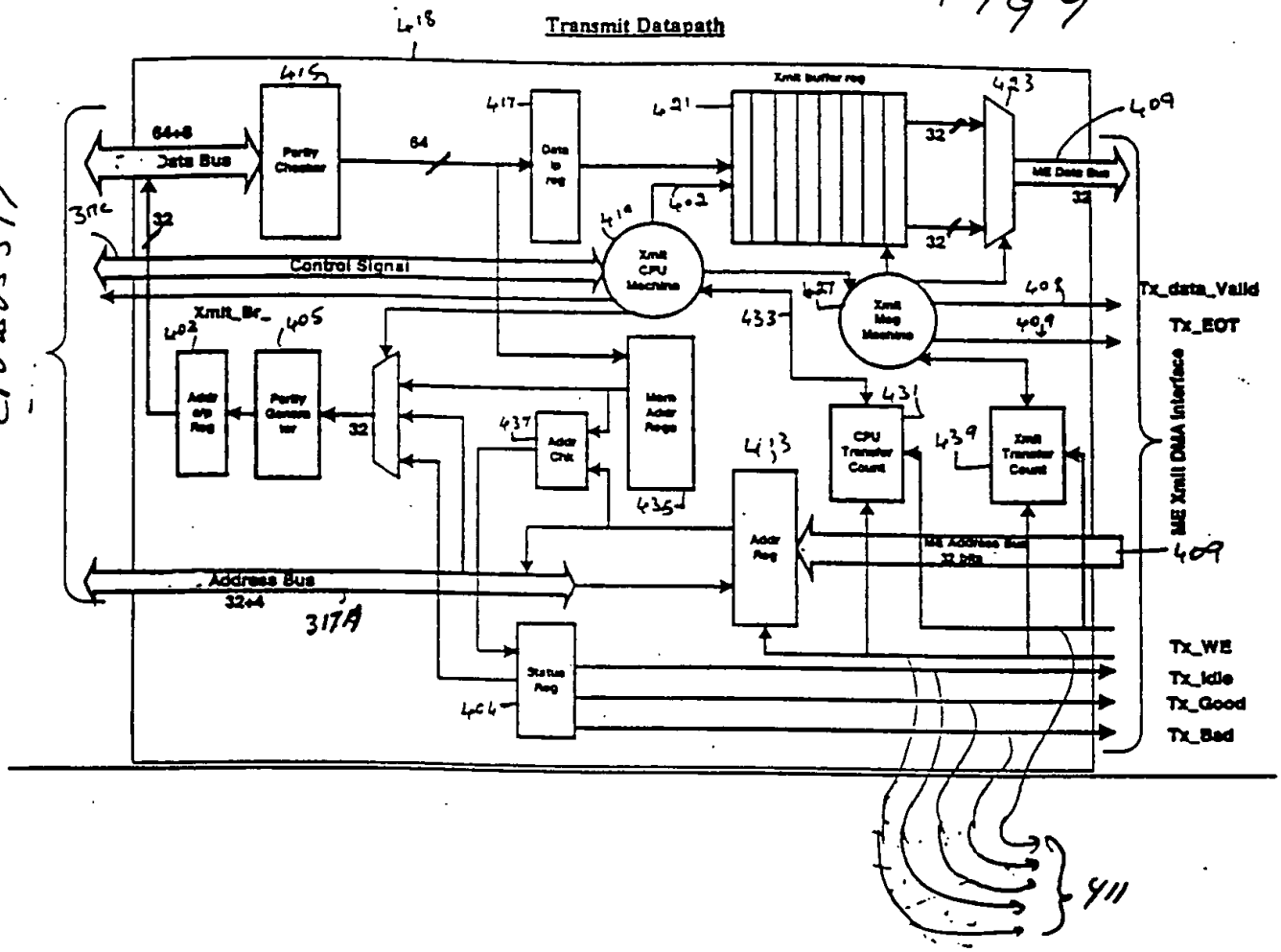
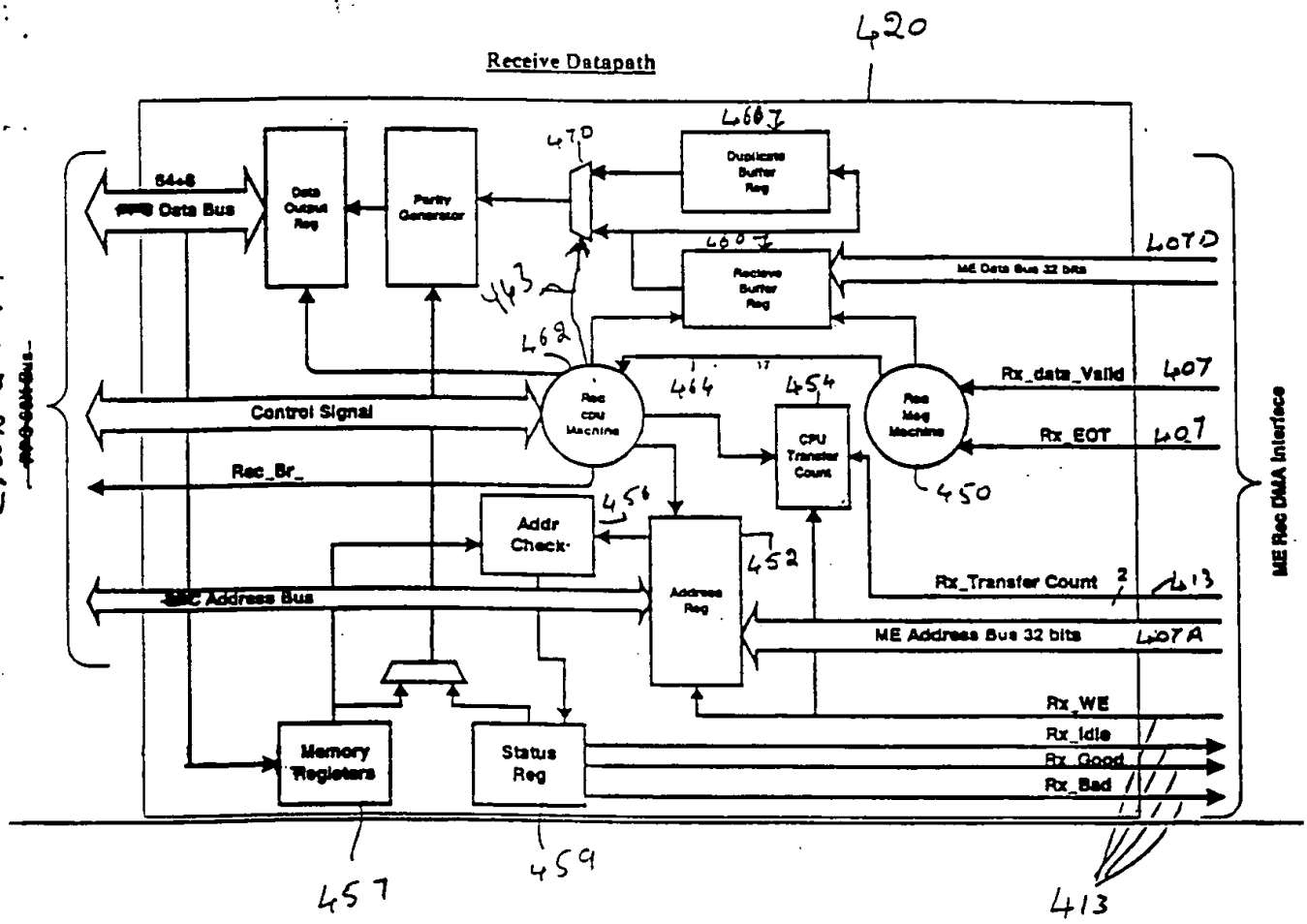

406A
SWITCH SECTION
FIFO
GENERATOR
ARBITER
436
449
M1
M2
M3
M4
SWITCH SECTION
SWITCH SECTION
SWITCH SECTION

FIG 9



CPU&VS317

FIG 10


420
Receive Datapath
Duplicate Buffer Reg
Data Output Reg
Parity Generator
Data Bus
Receive Buffer Reg
ME Data Bus 32 bits
Rx_data_Valid
Rx_EOT
Rec CPU Machine
Rec Msg Machine
CPU Transfer Count
Control Signal
Rec_Br_
Addr Check
Address Reg
Address Bus
Rx_Transfer Count
ME Address Bus 32 bits
Rx_WE
Rx_Idle
Rx_Good
Rx_Bad
Memory Registers
Status Reg
ME Rec DMA Interface
CPU BUS 317
457
459
413

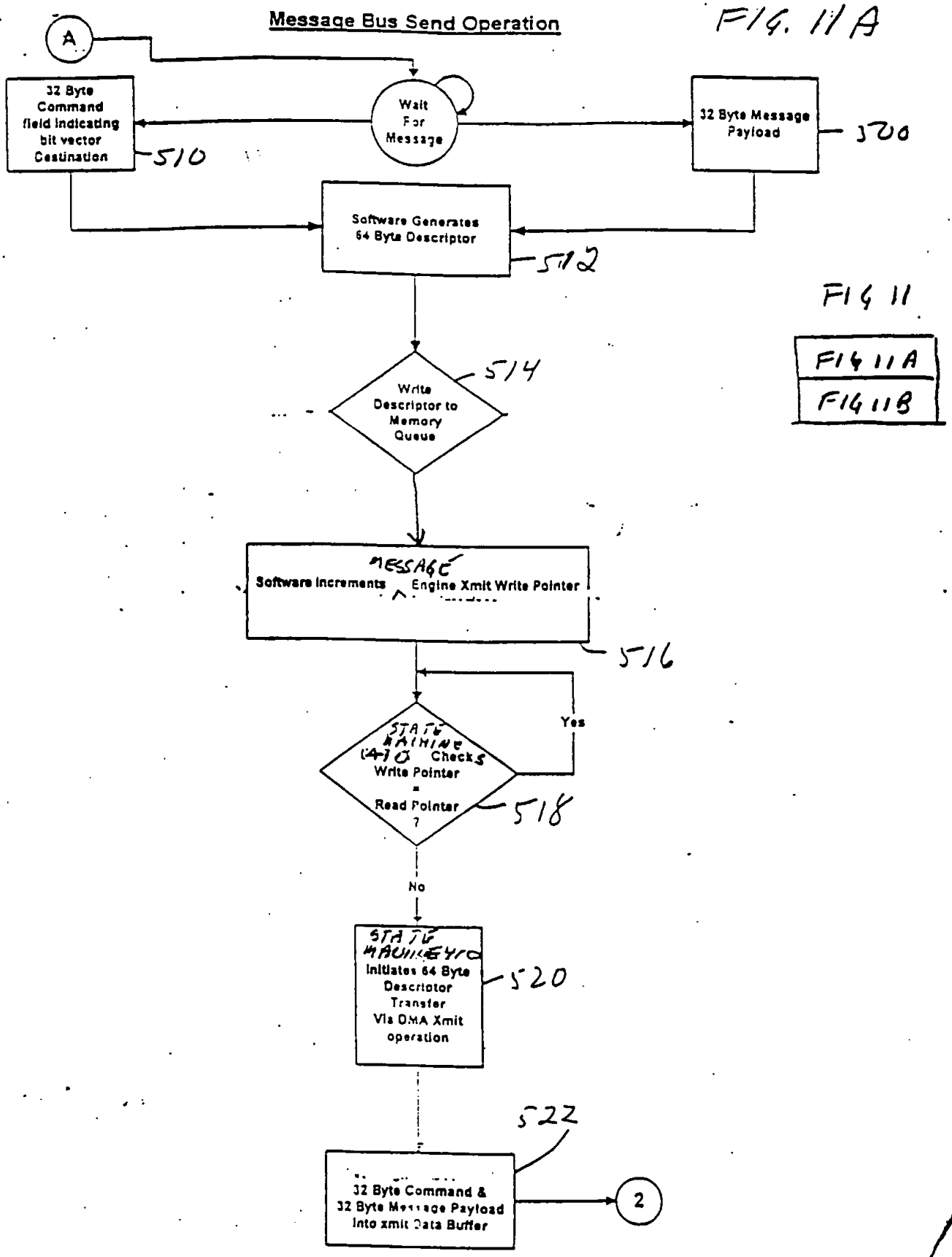


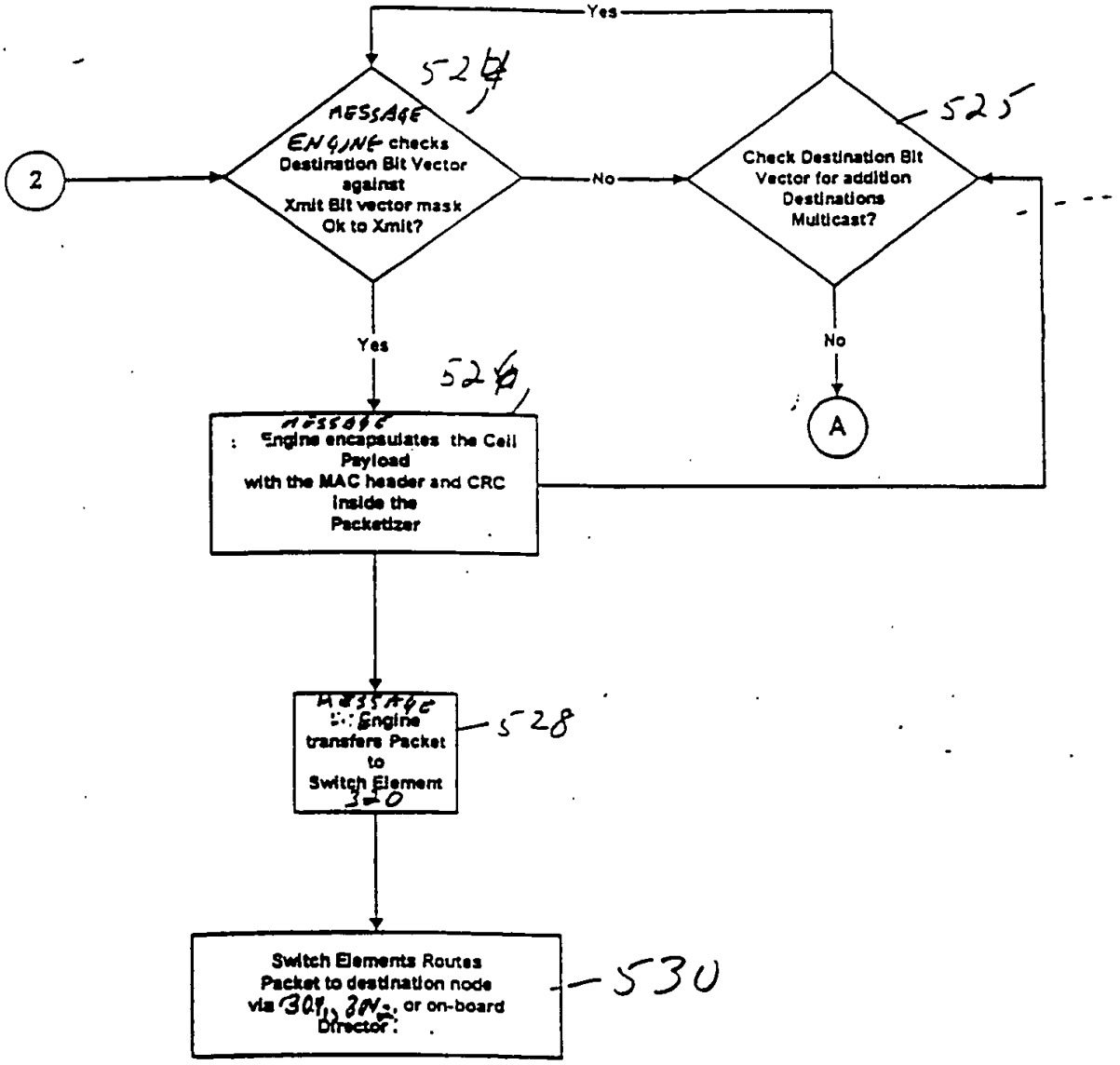
FIG. 11A

FIG 11

FIG 11A
FIG 11B

Message Bus Send Operation Continued

FIG 11B



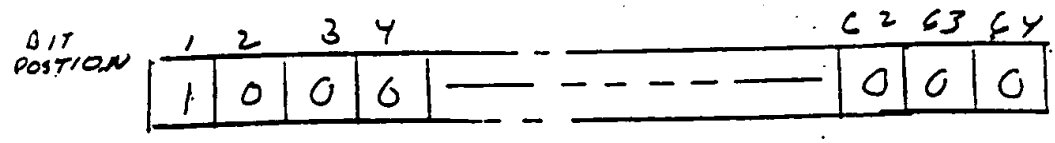


FIG 11C

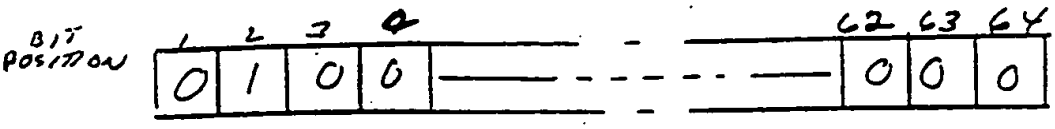


FIG 11D

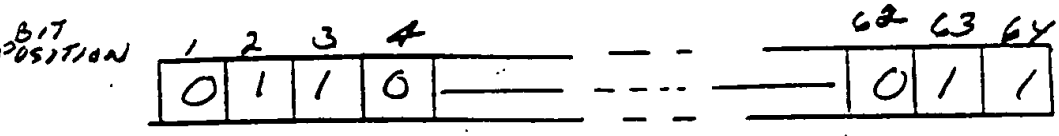


FIG 11E

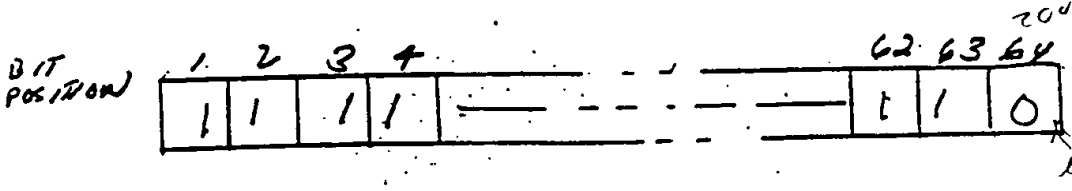


FIG 11F

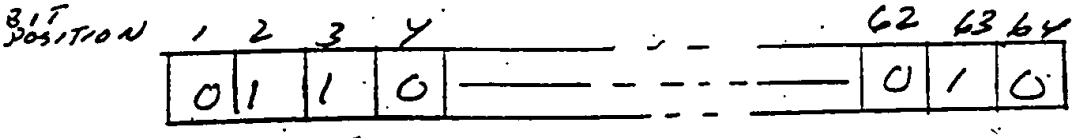


FIG 11G

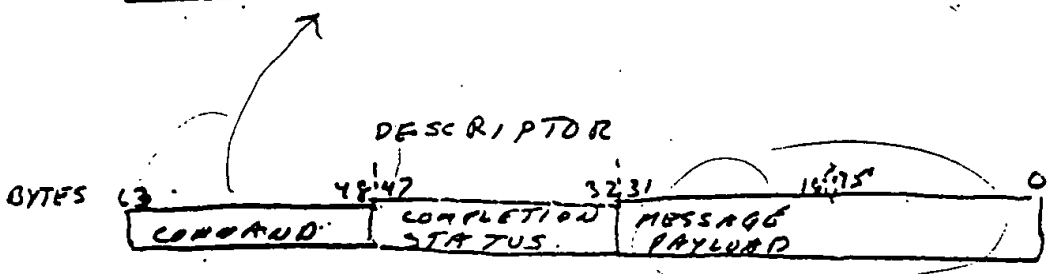


FIG 2A

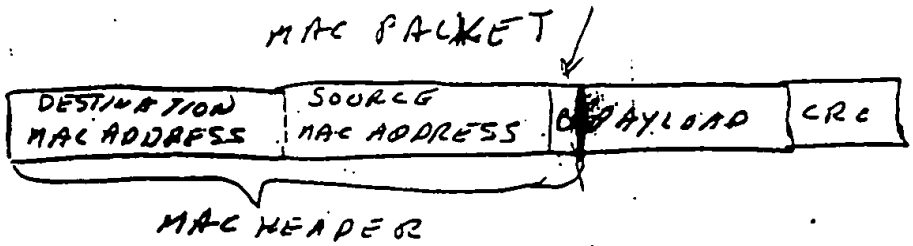


FIG 2B

Message Bus Receive Operation

FIG. 12A

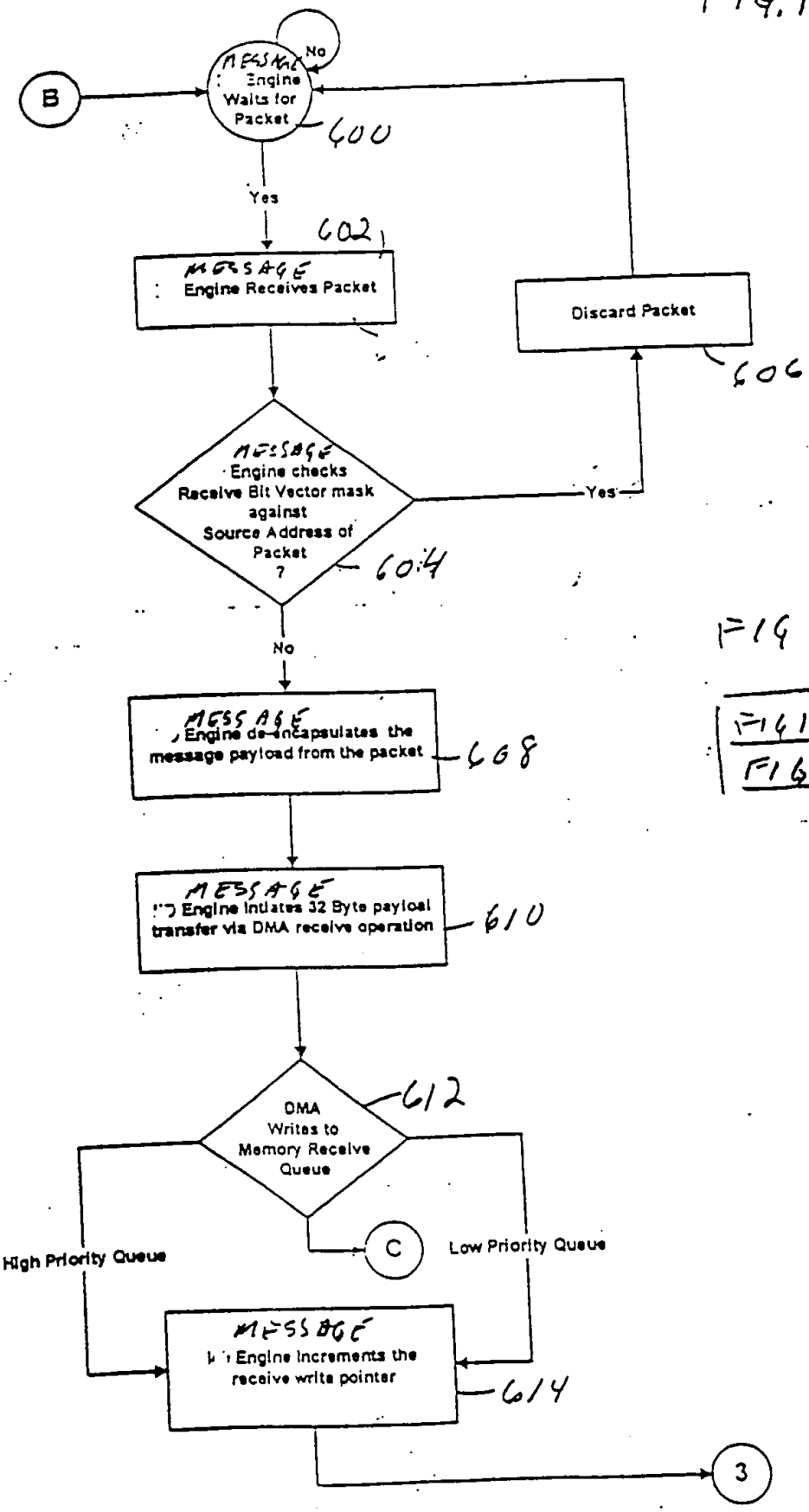


FIG 12

FIG 12A
FIG 12B

Message Bus Receive Operation Continued

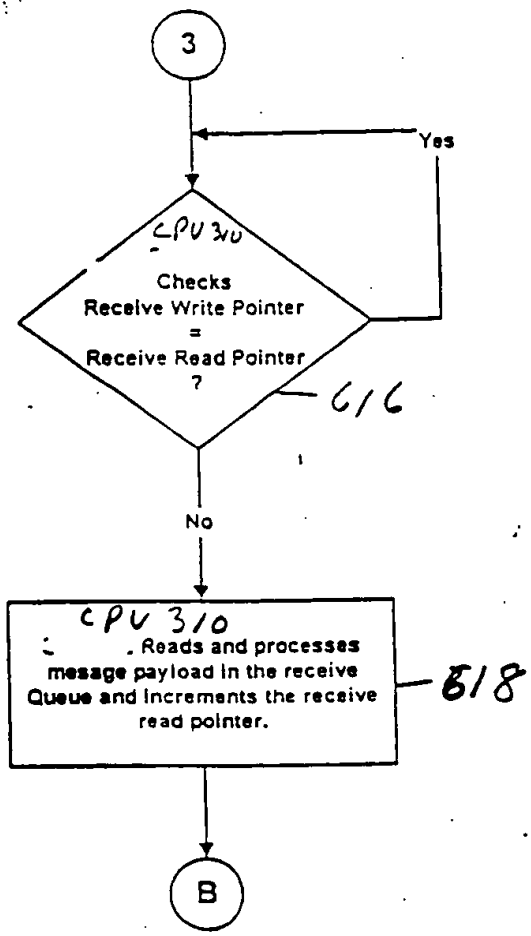


FIG 12B

Message Bus Acknowledgement Operation

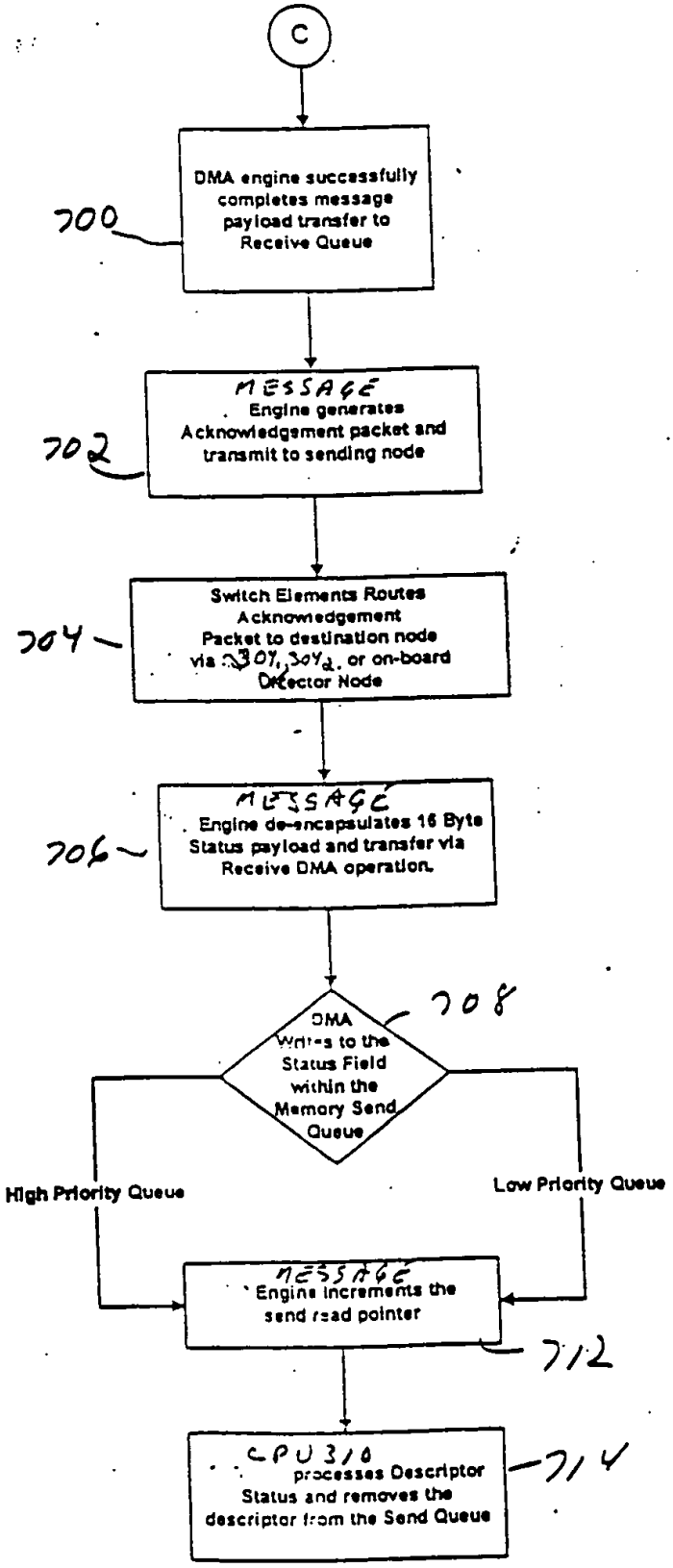
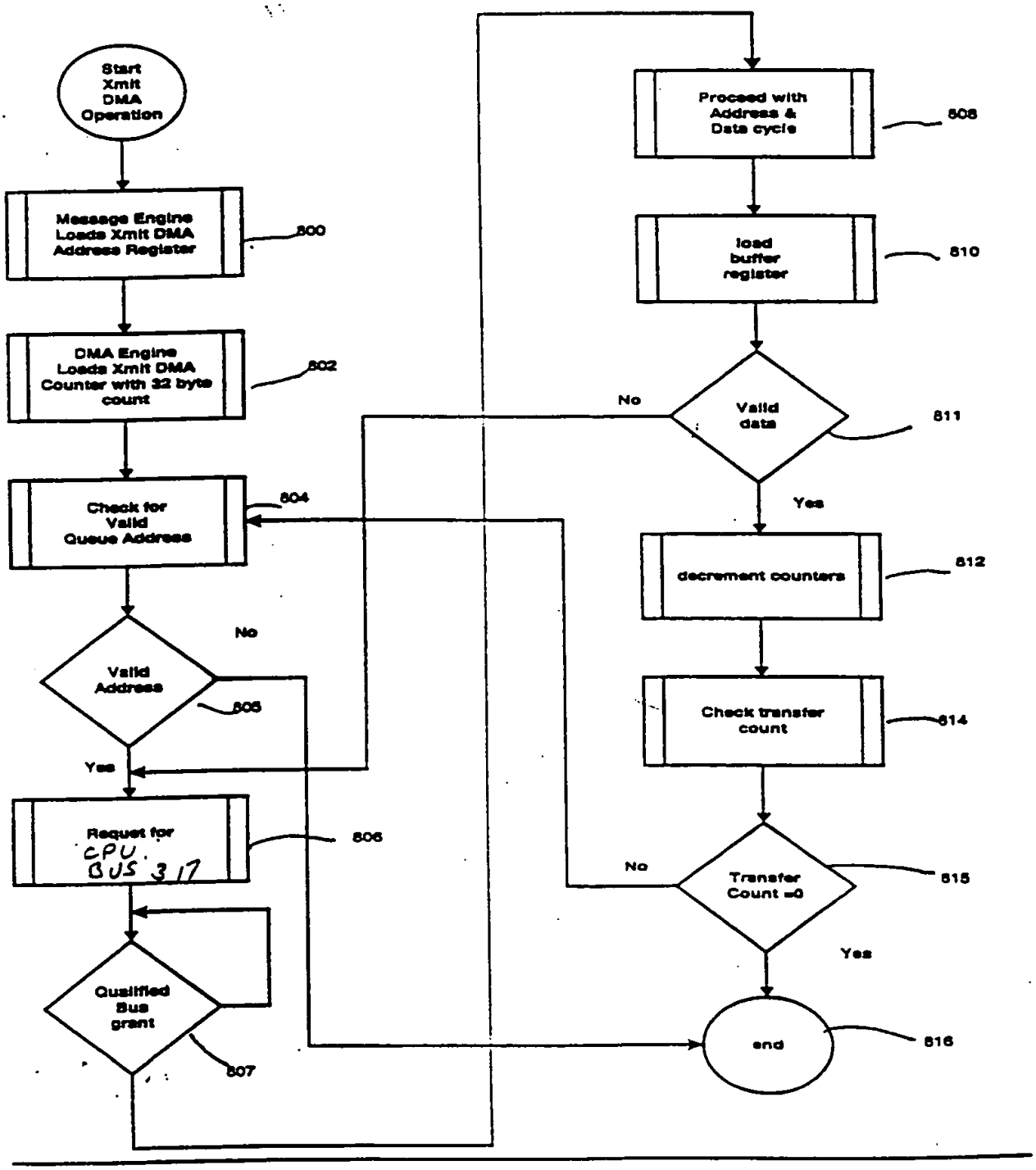


FIG. 13

FIG 4A

Xmit CPU flow



F-1414B

Xmit Msg flow

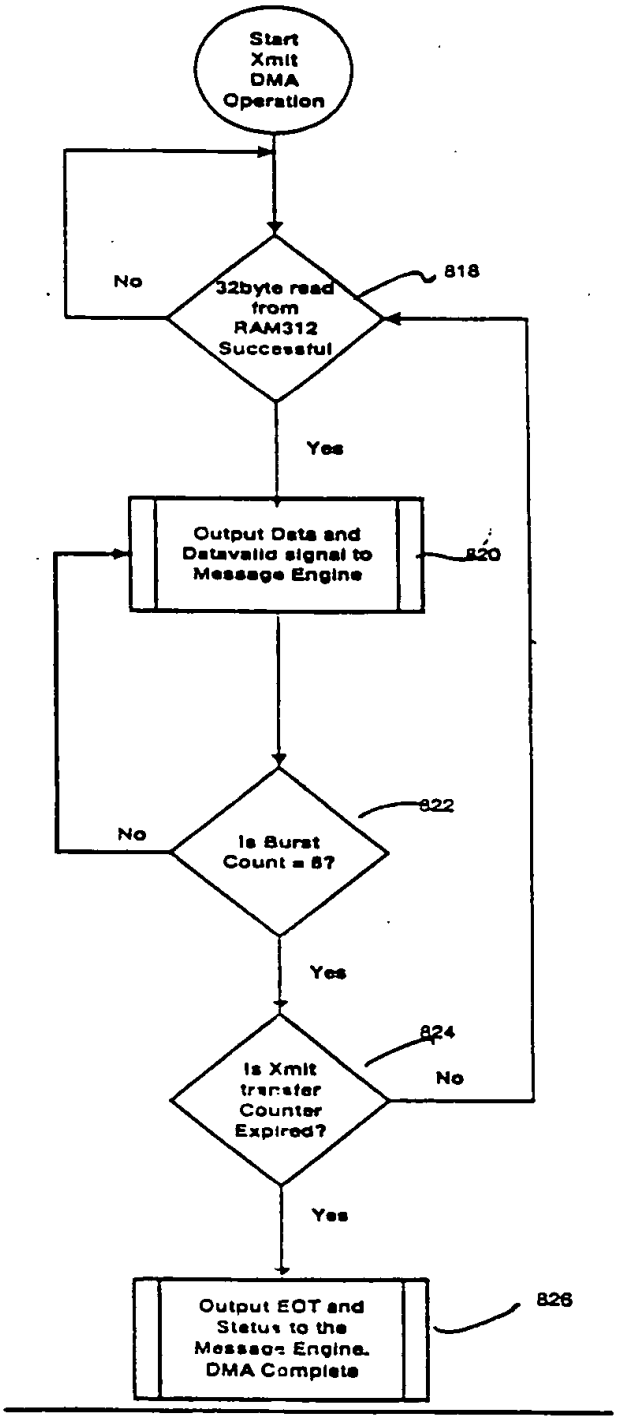
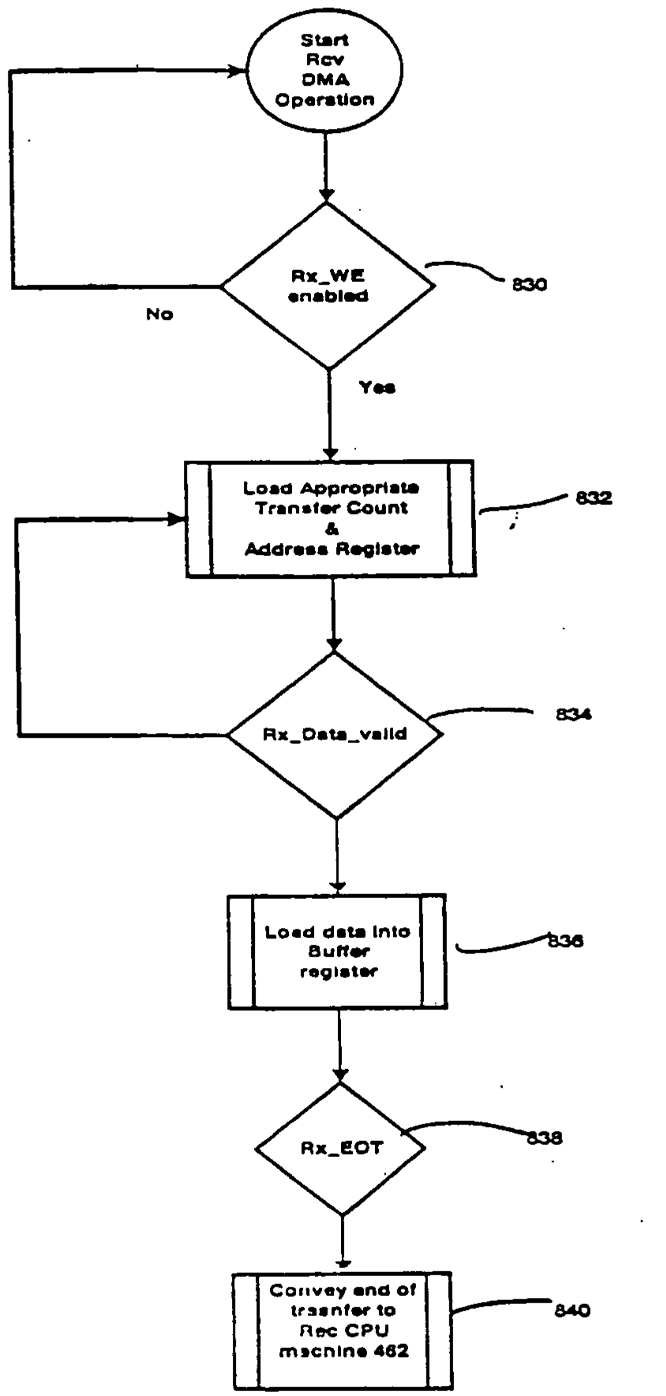


FIG 15A

Rec msg flow



09527100 . 031599

FIG 15B

Rec cpu flow

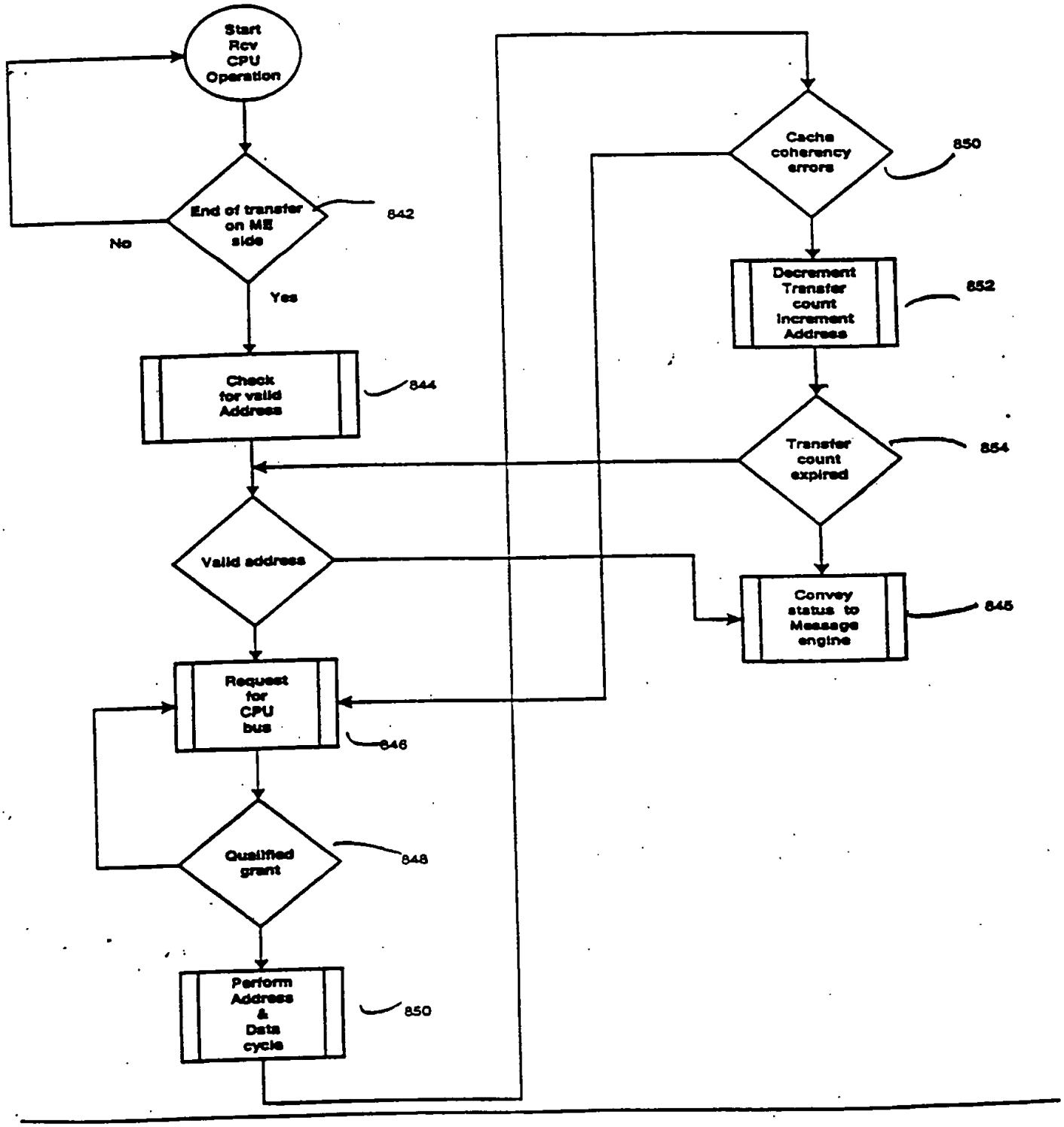


FIG 16

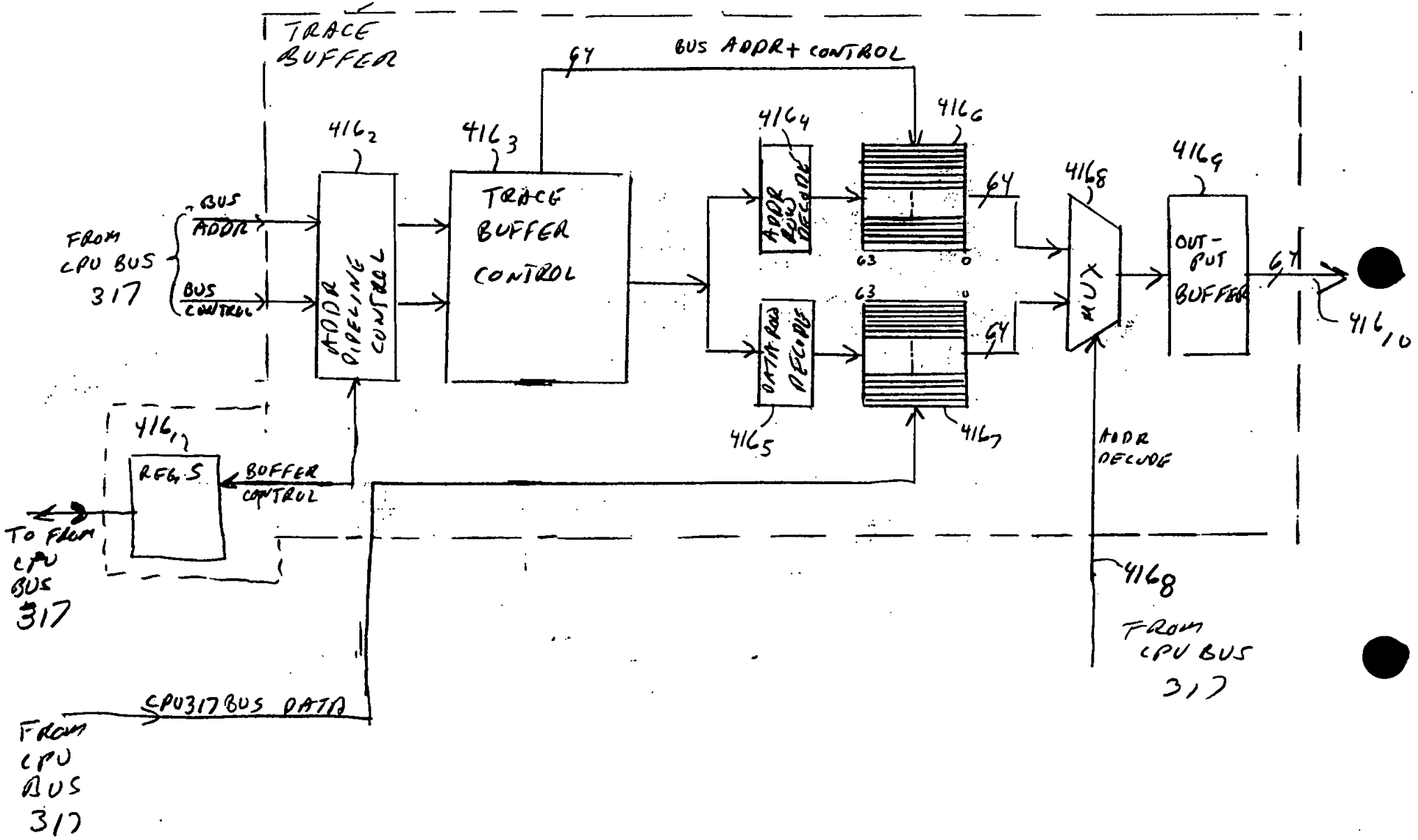

416
TRACE BUFFER
64
BUS ADDR + CONTROL
FROM CPU BUS 317
BUS ADDR
BUS CONTROL
416₂
ADDR PIPELINE CONTROL
416₃
TRACE BUFFER CONTROL
416₄
ADDR BUS DECODE
416₆
63
0
64
416₈
MUX
416₉
OUT-PUT BUFFER
64
416₁₀
DATA BUS DECODE
416₅
63
0
64
416₇
416₁₁
REGS
BUFFER CONTROL
TO FROM CPU BUS 317
ADDR DECODE
416₈
FROM CPU BUS 317
CPU 317 BUS DATA
FROM CPU BUS 317

FIG. 17

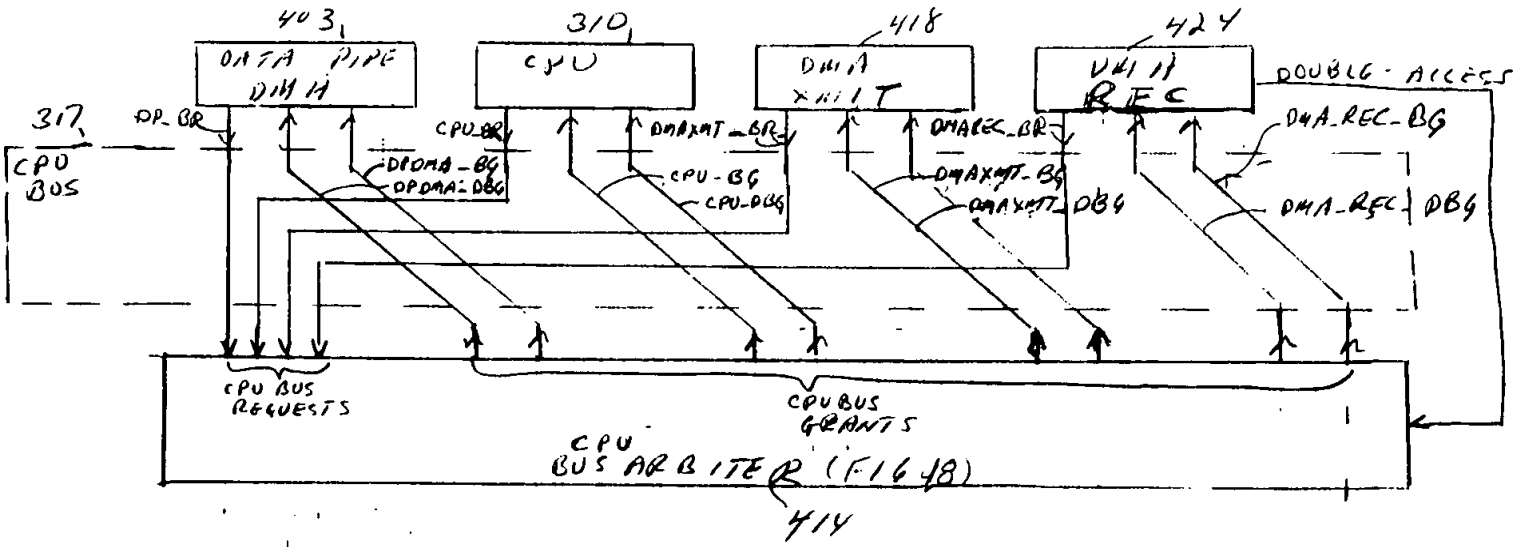

403
DATA PIPE DMA
310
CPU
418
DMA XMIT
424
DMA REC
DOUBLE-ACCESS
317
CPU BUS
DP_BR
CPU_BR
DMAXMT_BR
DMAREC_BR
DPDMA_BG
DPDMA_DBG
CPU_BG
CPU_DBG
DMAXMT_BG
DMAXMT_DBG
DMA_REC_BG
DMA_REC_DBG
CPU BUS REQUESTS
CPU BUS GRANTS
CPU BUS ARBITER (FIG 48)
414

FIG 18

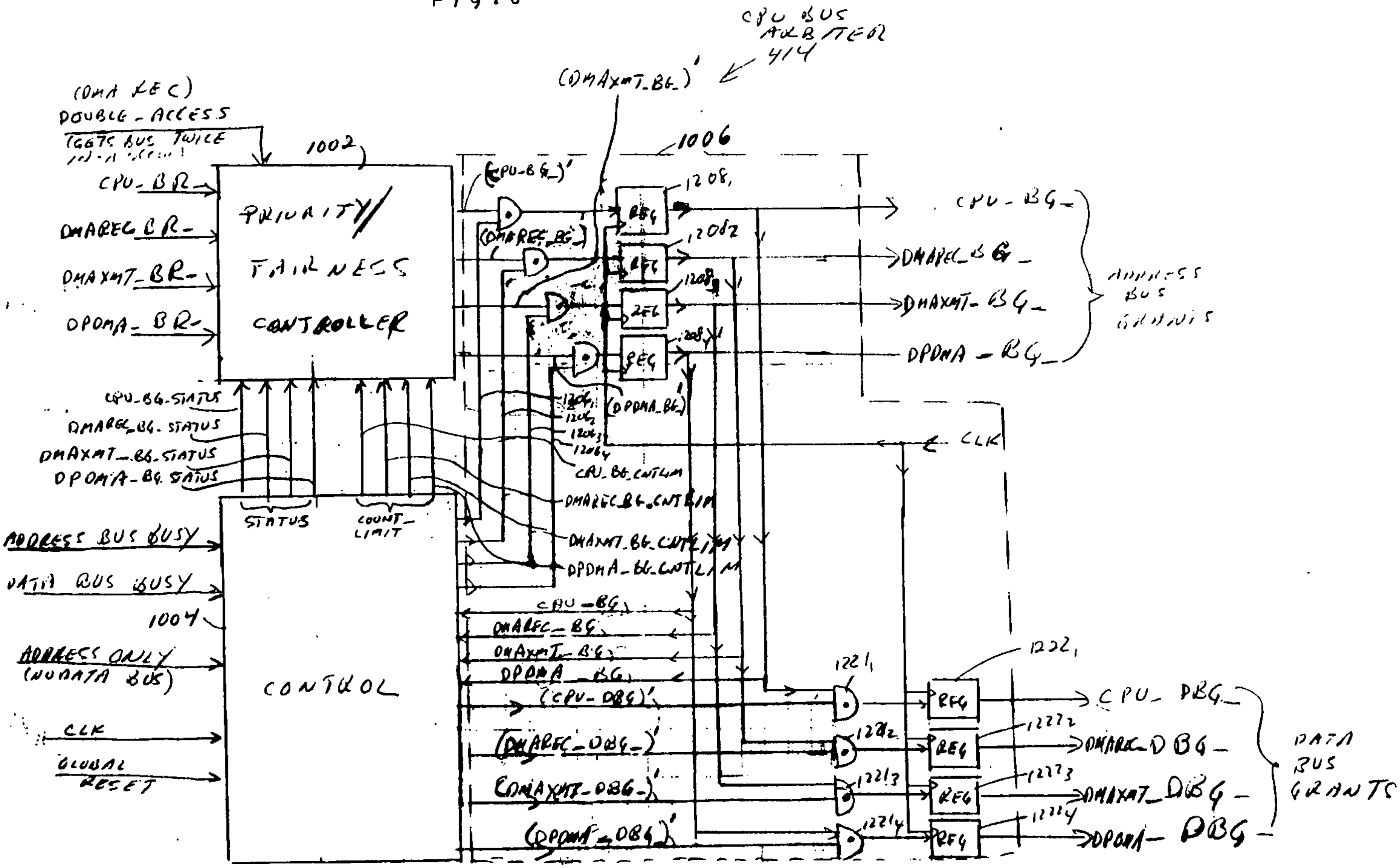

CPU BUS ARBITER 414
(DMAXMT_BG_)'
1006
1002
(DMA REC) DOUBLE_ACCESS
CPU_BR_
DMAREC BR_
DMAXMT_BR_
DPDMA_BR_
PRIORITY/ FAIRNESS CONTROLLER
(CPU-BG_)'
(DMAREC_BG_)'
REG
1208₁
1208₂
1208₃
1208₄
CPU_BG_
DMAREC_BG_
DMAXMT_BG_
DPDMA_BG_
(DPDMA_BG_)'
CPU_BG_STATUS
DMAREC_BG_STATUS
DMAXMT_BG_STATUS
DPDMA_BG_STATUS
1206₁
1206₂
1206₃
1206₄
CPU_BG_CNTLIM
DMAREC_BG_CNTLIM
DMAXMT_BG_CNTLIM
DPDMA_BG_CNTLIM
CLK
STATUS
COUNT_LIMIT
ADDRESS BUS BUSY
DATA BUS BUSY
1004
ADDRESS ONLY (NO DATA BUS)
CLK
GLOBAL RESET
CONTROL
CPU_BG_
DMAREC_BG_
DMAXMT_BG_
DPDMA_BG_
(CPU_DBG_)'
(DMAREC_DBG_)'
(DMAXMT_DBG_)'
(DPDMA_DBG_)'
1221₁
1221₂
1221₃
1221₄
1222₁
1222₂
1222₃
1222₄
CPU_DBG_
DMAREC_DBG_
DMAXMT_DBG_
DPDMA_DBG_
DATA BUS GRANTS

FIG. 19

POTENTIAL GRANT TO: →	CPU_BR	DMAREC_BR	DMAXMT_BR	DPDMA_BR	CPU_BG STATUS	DMAREC_BG STATUS	DMAXMT_BG STATUS	DPDMA_BG STATUS	CPU_BG_CNTLIM	DMAREC_BG_CNTLIM	DMAXMT_BG_CNTLIM	DPDMA_BG_CNTLIM	DOUBLE-ACCESS
(CPU_BG)'	DC	0	0	0	DC	DC	DC	DC	DC	DC	DC	DC	DC
(CPU_BG)'	1	DC	DC	DC	0	DC	DC	DC	DC	0	0	0	0
(CPU_BG)'	1	DC	DC	DC	DC	DC	DC	DC	1	DC	DC	DC	0
(DMAREC_BG)'	0	1	0	0	DC	DC	DC	DC	DC	DC	DC	DC	DC
(DMAREC_BG)'	DC	1	DC	DC	DC	1	DC	DC	DC	DC	DC	DC	1
(DMAREC_BG)'	0	1	DC	DC	DC	0	DC	DC	DC	DC	0	0	DC
(DMAREC_BG)'	1	1	DC	DC	1	DC	DC	DC	0	DC	0	0	DC
(DMAREC_BG)'	DC	1	DC	DC	DC	DC	DC	DC	0	1	DC	DC	DC
(DMAXMT_BG)'	0	0	1	0	DC	DC	DC	DC	DC	DC	DC	DC	DC
(DMAXMT_BG)'	0	0	1	DC	DC	DC	0	DC	DC	DC	DC	0	DC
(DMAXMT_BG)'	0	1	1	DC	DC	1	DC	DC	DC	DC	DC	0	0
(DMAXMT_BG)'	1	0	1	DC	1	DC	DC	DC	DC	DC	DC	0	DC
(DMAXMT_BG)'	DC	DC	1	DC	DC	DC	DC	DC	0	0	1	DC	0
(DPDMA_BG)'	0	0	0	1	DC	DC	DC	DC	DC	DC	DC	DC	DC
(DPDMA_BG)'	0	0	1	1	DC	DC	1	0	DC	DC	DC	DC	DC
(DPDMA_BG)'	0	1	0	1	DC	1	DC	DC	DC	DC	DC	DC	0
(DPDMA_BG)'	1	0	0	1	1	DC	DC	DC	DC	DC	DC	DC	DC
(DPDMA_BG)'	DC	DC	DC	1	DC	DC	DC	DC	0	0	0	1	0

FIG 20

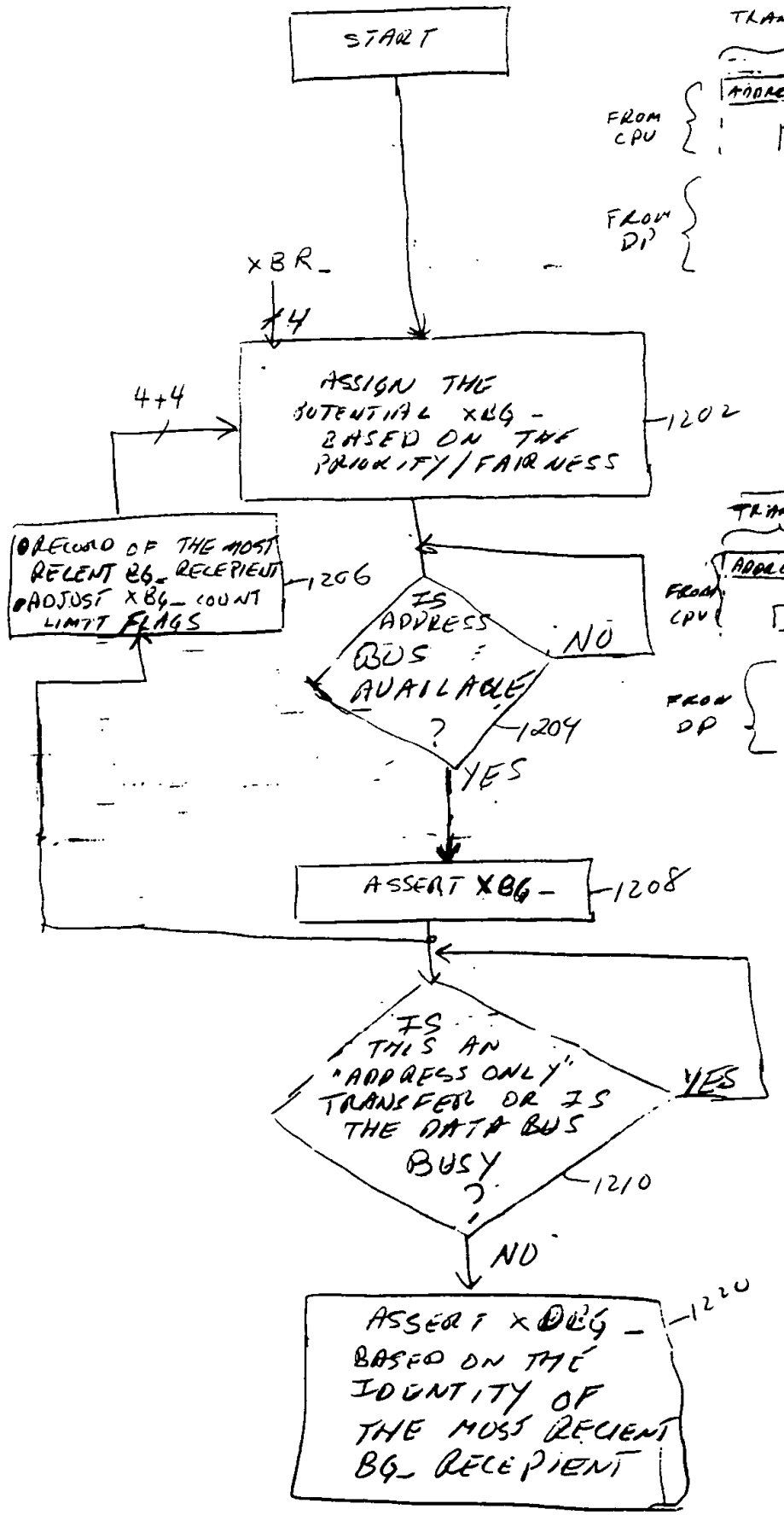


FIG 21A

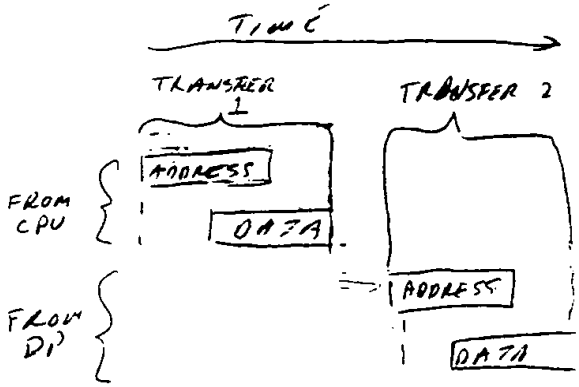


FIG 21B

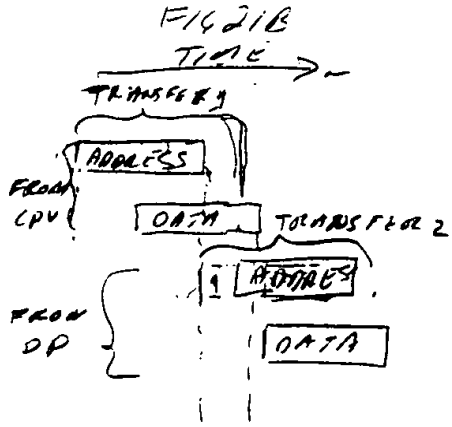
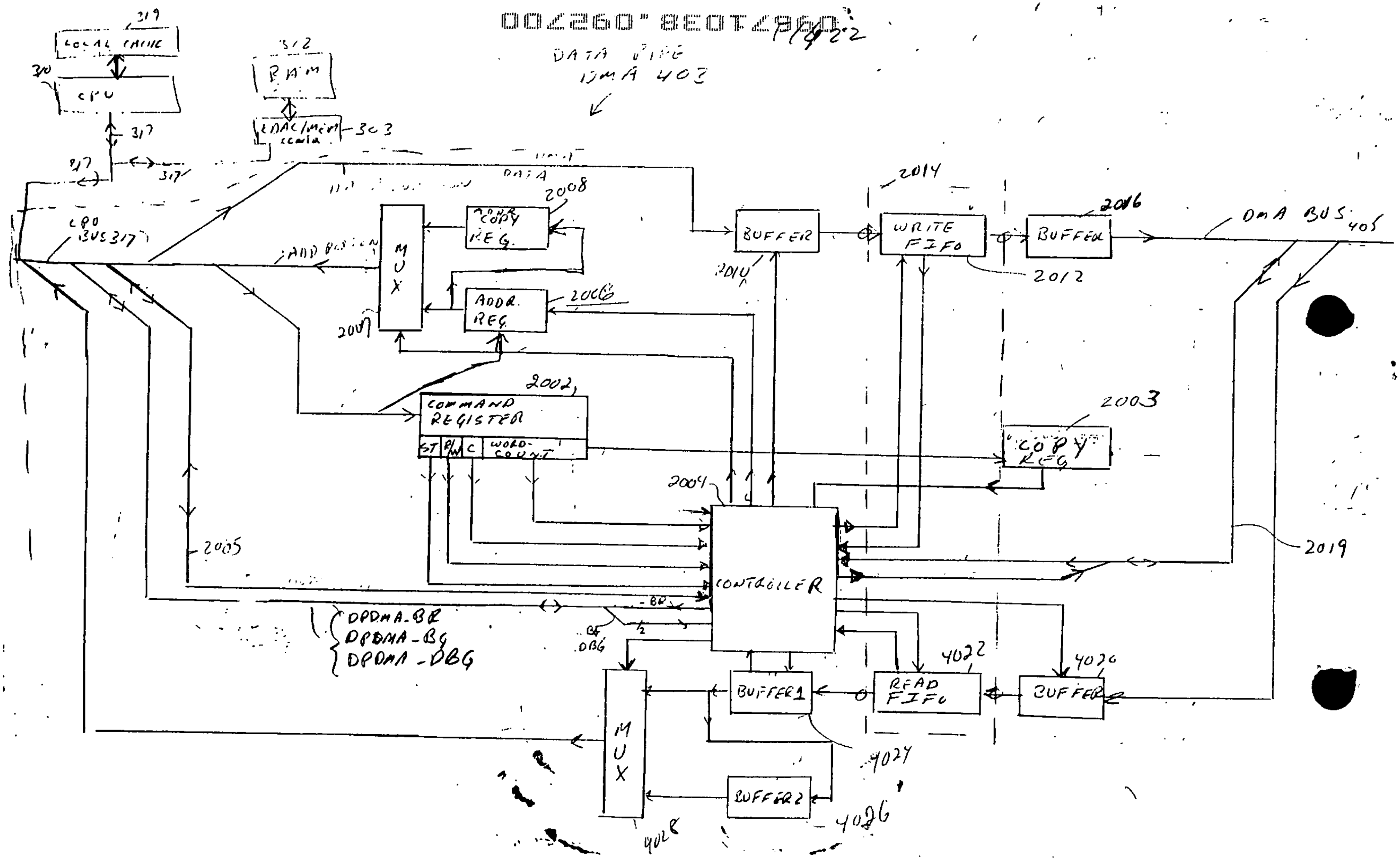


FIG 22


DATA PIPE
DMA 402
319
LOCAL CACHE
310
CPU
312
RAM
EDAC/MEM CNTR
303
317
CPU BUS 317
2008
COPY REG.
MUX
2007
ADDR. REG.
2006
2002
COMMAND REGISTER
ST
R/W
C
WORD-COUNT
2005
DPDMA-BR
DPDMA-BG
DPDMA-DBG
BR
BG
DBG
2004
CONTROLLER
BUFFER
2010
2014
WRITE FIFO
2012
BUFFER
2016
DMA BUS 405
2003
COPY REG
2019
READ FIFO
4022
BUFFER
4020
BUFFER1
4024
BUFFER2
4026
MUX
4028